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Deep level defects in n-type GaAsBi and GaAs grown at low temperatures

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Deep level defects in n-type $GaAs_{1-x}Bi_x$ having $0 < x < 0.012$ and GaAs grown by molecular beam epitaxy (MBE) at substrate temperatures between 300 and 400 °C have been investigated by Deep Level Capacitance Spectroscopy. Incorporating Bi suppresses the formation of an electron trap with activation energy 0.40 eV, thus reducing the total trap concentration in dilute GaAsBi layers by more than a factor of 20 compared to GaAs grown under the same conditions. We find that the dominant traps in dilute GaAsBi layers are defect complexes involving As_{Ga}, as expected for MBE growth at these temperatures. © *2013 American Institute of Physics*.
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INTRODUCTION

$GaAs_{1-x}Bi_x$ alloys are of interest because of their potential to improve the properties of conventional III–V semiconductor devices and to extend them to longer infrared wavelengths.[1–3] The bandgap energy of $GaAs_{1-x}Bi_x$ alloys decreases strongly as the Bi fraction is increased and is predicted to be zero when the Bi fraction reaches $x \approx 0.35$.[1] In addition, the lattice constant increase of $GaAs_{1-x}Bi_x$ is much smaller than that of $In_xGa_{1-x}As$ at the same bandgap energy,[1] thus considerably reducing constraints related to lattice mismatch strain for $GaAs_{1-x}Bi_x$/GaAs heterostructures. Strong photoluminescence[4] and electroluminescence from thin $GaAs_{1-x}Bi_x$ layers located at the center of the *i*-region in *p-i-n* diodes[5] were recently reported. Other properties of this new semiconductor alloy, such as the increased spin-orbit coupling and the separation of the split-off hole band that exceeds the bandgap energy when $x > 0.09$, offer potential advantages for spintronic devices and long wavelength lasers, respectively.[6,7]

Bi is incorporated into undoped GaAs films grown by molecular beam expitaxy (MBE) only at growth temperatures below about 400 °C.[8–10] Infrared absorption measurements of undoped GaAs layers grown by MBE at 400 °C and 325 °C have shown high concentrations, $\sim 10^{18}\,cm^{-3}$, of a defect complex involving As on a Ga lattice site (As_{Ga}).[11] Temperature dependent Hall effect measurements of similar un-doped GaAs layers grown at 400 °C revealed a deep donor, which involves As_{Ga} and has an activation energy 0.65 eV below the conduction band, at a concentration of $2 \times 10^{17}\,cm^{-3}$.[12] The dominant electron trap in Deep Level Capacitance Spectroscopy (DLTS) spectra of Si-doped layers grown by MBE at 450 °C also has activation energy 0.65 eV, but the trap concentration is lower, about $3 \times 10^{16}\,cm^{-3}$.[13] Similarly, the activation energy of the dominant trap in DLTS spectra of *p-i-n* diodes having intrinsic regions consisting of both GaAs and GaAsBi (1.4-1.8%Bi) layers is 0.63 eV.[14] In these structures the trap concentrations were lower, increasing from $1 \times 10^{15}\,cm^{-3}$ in the structure grown at 350 °C to $7 \times 10^{15}\,cm^{-3}$ in the structure grown at 310 °C. Taken together, these results suggest that defect concentrations, and perhaps also defect species, in MBE layers grown in the temperature range 300–450 °C depend sensitively on other growth conditions as well, not only on the growth temperature.

To further investigate defects in dilute GaAsBi alloys, we have performed DLTS measurements on *n*-type $GaAs_{1-x}Bi_x$ layers having $0 \le x \le 0.011$ grown by MBE at substrate temperature 330 °C and also n-type GaAs layers grown at 330 °C and 390 °C. The dominant electron trap in GaAs grown at 330 °C has emission activation energy 0.40 eV and concentration $10^{18}\,cm^{-3}$. When only 0.3% Bi is incorporated into GaAs at 330 °C, the formation of the 0.40 eV trap is suppressed completely. Other electron traps, including one having activation energy 0.65 eV, are present in both the GaAs and $GaAs_{1-x}Bi_x$ layers and, therefore, originate from MBE growth at low temperatures.

EXPERIMENT

Epitaxial layer structures for *p*+/*n* diodes (see Fig. 1) were grown by MBE on Si-doped GaAs (001) substrates for DLTS measurements. Ga-type effusion cells were used for Ga and Bi, and an As cracker was used for As_2. The *n*-type dopant is Si from a solid Si source and the *p*-type dopant is C from a CBr_4 source. The heavily doped GaAs buffer and capping layers were grown at standard conditions (substrate temperature 580 °C, As/Ga atom ratio 6, growth rate 1 μm/h). To grow the GaAsBi layers, the As/Ga atom ratio and substrate temperature were reduced abruptly to ~2 and 330 °C,

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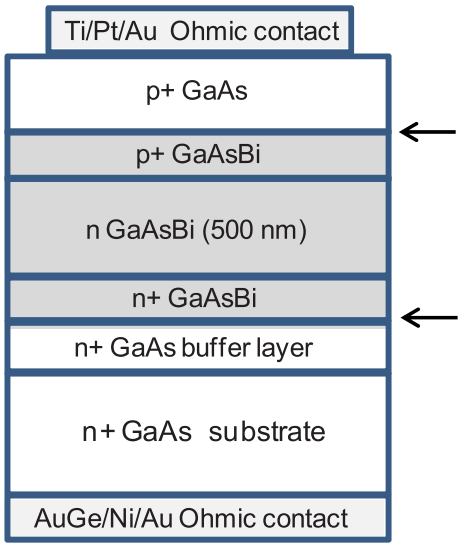

FIG. 1. Diagram showing the layer structure of asymmetric p+/n diodes for DLTS measurements of n-type $GaAs_{1-x}Bi_x$ layers. The arrows indicate where substrate temperature changes were made to achieve abrupt heterointerfaces between the GaAs and GaAsBi layers.

respectively, and a Bi flux, varied to yield different alloy compositions, was added, while maintaining the growth rate of 1 μm/h. In this way abrupt $GaAs_{1-x}Bi_x$/GaAs heterointerfaces were formed within the heavily doped n+ and p+ contact layers above and below the *n*-doped GaAsBi layer. The Bi fraction, shown in Table I, was determined by high resolution x-ray diffraction measurements.[1] For comparison, pure GaAs structures were also grown: one with GaAs grown under the same conditions as the GaAsBi layers, but with no Bi flux, and another consisting entirely of GaAs layers grown under standard conditions. Atomic force microscopy (AFM) showed that all the samples have smooth surfaces. Although long straight surface steps that are typically associated with misfit dislocation glide were detected on the surface of the 0.7% GaAsBi sample, the density was low (3–13 on a 50 μm × 50 μm image) and no strain relaxation of the GaAsBi layers was detected by XRD. To avoid dislocation glide at higher lattice mismatch strain, the p+ GaAs cap layer of the 1.1% GaAsBi sample was grown at 400 °C rather than at the standard growth temperature and AFM showed no evidence of dislocation formation.

TABLE I. Growth temperature, Bi fraction, As/Ga atom ratio, growth rate, and net donor concentration of the n-type layer in samples prepared for DLTS measurements. All devices are asymmetric p+/n junction diodes except for the GaAs Schottky diode grown at 390 °C. The doping concentration is from capacitance-voltage measurements at 300 K.

Growth Temp. (°C)	% Bi	As/Ga atom ratio	N_d-N_a (cm^{-3})
580	0	6	9×10^{16}
390[a]	0	3	3×10^{16}
330	0	1.7	2×10^{17}
330	0.3	1.9	6×10^{16}
330	0.7	1.7	4×10^{16}
330	1.1	2.0	5×10^{16}

[a]Si dopant source was $SiBr_4$.

The p+/n diodes were fabricated with large area Ni/AuGe/Au Ohmic contacts on the back side of the Si-doped substrate and 400 μm-diameter Ti/Pt/Au Ohmic contacts to the *p*+ GaAs cap layer that were alloyed at 450 °C for 30 s. The devices were isolated by mesa etching to a depth below the p+/n interface, typically about 2 μm. In addition, 400 μm-diameter Cr/Au Schottky contacts were deposited on a Si-doped GaAs layer grown at 390 °C with an As/Ga atom ratio of 3 on a heavily n-doped GaAs buffer layer grown at standard conditions on an n-type GaAs substrate. For this sample a large area Cr/Au film served as a low resistance tunnel contact on the back side of the Si-doped GaAs substrate.

The net donor concentration in the n-doped layer was determined from capacitance-voltage (C–V) measurements. From the principle of detailed balance, an electron is thermally emitted from a deep level to the bottom of the conduction band at a rate given by

$$e_n = \sigma_n v_n N_c \exp(-E_A/kT), \tag{1}$$

where the thermal emission activation energy is $E_A = E_C - E_T$, σ_n is the electron capture cross section, v_n is the electron thermal velocity, and N_C is the conduction band density of states. In the DLTS measurement, the diode is reverse biased at V_R and short trap filling pulses at voltage V_P are applied repeatedly as the sample temperature is scanned. Electron (or hole) emission from energy levels in the depletion region is detected as a capacitance transient following each filling pulse. A peak in the DLTS signal is observed, when the thermal emission rate is equal to the rate window set on the spectrometer. The thermal emission activation energy and capture cross section for each deep level defect were determined in the usual way from the slope and intercept of Arrhenius plots of T^2/e_n vs. $1000/T$, where T is the temperature of the DLTS peak and e_n is the spectrometer rate window. The trap concentration, N_T, was calculated from the magnitude of the DLTS peak, ΔC, with the relation

$$N_T = 6N_d \left| \frac{\Delta C}{C(V_R)} \right| \left\{ \frac{W^2(V_R)}{\left(W(V_R) - \lambda\right)^2 - \left(W(V_p) - \lambda\right)^2} \right\}, \tag{2}$$

where N_d is the net donor concentration, $C(V_R)$ is the capacitance at reverse bias, $C(V_P)$ is the capacitance at the trap filling voltage, and W is the depletion width. These parameters were determined from C–V measurements at the temperature of the DLTS peak.

$$\lambda = \left\{ \frac{2\varepsilon}{e^2 N_d} (E_F - E_T) \right\}^{1/2}, \tag{3}$$

is the distance within the depletion region, where the traps do not emit electrons because the trap energy level (E_T) lies below the Fermi energy (E_F), as shown in Fig. 2. When the reverse bias leakage current is relatively large, especially at the higher temperatures of the DLTS scan, requiring measurements to be made with a small value of V_R, the term in

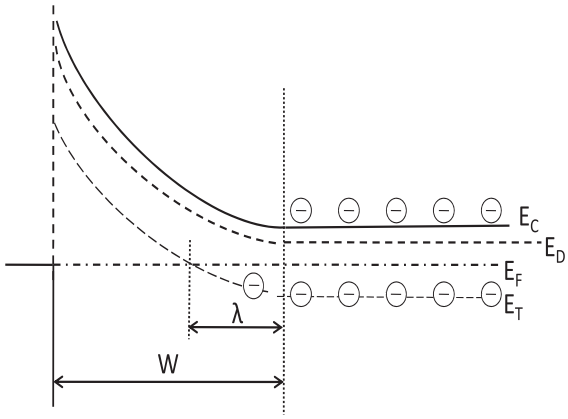

FIG. 2. Band diagram of an *n*-type Schottky diode at zero applied voltage with the conduction band energy, E_C, the donor energy, E_D, the Fermi energy, E_F, and a trap energy, E_T, indicated. W is the depletion width and λ indicates the distance from the edge of the depletion region to the point, where $E_T = E_F$. Traps within the distance λ of the depletion edge at reverse bias do not contribute to the DLTS signal.

brackets in Eq. (2) can be as large as ~10 for mid-gap traps. The factor of 6 in Eq. (2) comes from the relationship between the amplitude of the capacitance transient immediately following the filling pulse and the DLTS peak amplitude with our SULA Technologies spectrometer. A general calculation for the latter can be found in Ref. 15.

RESULTS AND DISCUSSION

DLTS spectra for three Si-doped GaAs samples grown at different temperatures are shown in Fig. 3. The concentrations of three traps with properties similar to the M1, M3, and M4 traps, typically seen in GaAs grown at standard conditions,[16] are $\leq 4 \times 10^{13}\,cm^{-3}$. However, when the growth temperature is reduced to 390 °C, trap concentrations become significant, as high as $10^{16}\,cm^{-3}$, as shown in Table

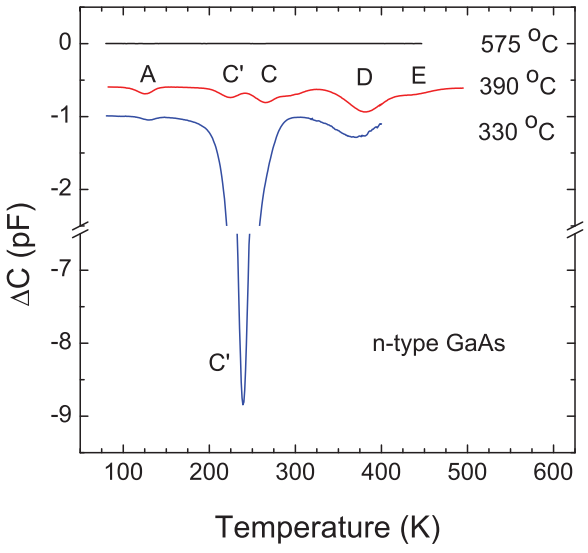

FIG. 3. DLTS spectra for n-type GaAs layers grown at three different substrate temperatures as indicated. The emission rate is $1163\,s^{-1}$. The trap filling pulse was 0.5 V forward bias for 2 ms. The steady state reverse bias voltage was 0.5 V for the layers grown at 580 °C and 390 °C and 0.2 V for the layer grown at 330 °C.

II. The DLTS spectrum for the GaAs layer grown at 330 °C shows that the DLTS peak of the 0.40 eV trap (trap C′) increased by more than a factor of 10, when the growth temperature was reduced from 390 °C. Consistent with this very large DLTS peak, the diode capacitance increases strongly with increasing temperature for T > 250 K. The net donor concentration calculated from C–V curves, increases as well and is $\sim 10^{18}\,cm^{-3}$ at 400 K. Above ~300 K, the emission rate of electrons in the C′ traps can follow the 1 MHz test signal and contribute to the capacitance measurement.[17] Therefore, the concentration of the 0.40 eV trap must be $\sim 10^{18}\,cm^{-3}$. The presence of such a high concentration of deep donor states modifies the calculation of the trap D concentration as discussed in the Appendix. Because the reverse bias leakage current increased at higher temperatures, measurements could not be made in the temperature range, where trap E would be detected. Trap C with activation energy 0.57 eV was not detected in this sample presumably because this DLTS peak is overwhelmed by the strong peak of the 0.40 trap. Both the different growth temperatures and different V/III atom ratios may contribute to the differences in the DLTS spectra of these three samples.

DLTS spectra for several $GaAs_{1-x}Bi_x$ samples are shown in Fig. 4 together with the spectrum for the GaAs sample grown at 390 °C. It is immediately obvious that incorporating Bi suppresses the formation of trap C′ in the 0.3% and 0.7% Bi samples, thus reducing deep level defect concentrations in GaAsBi layers grown at 330 °C by more than an order of magnitude to values in the mid $10^{16}\,cm^{-3}$ range. Due to the strong tendency for Bi to surface segregate, growth of GaAsBi alloys typically involves a Bi surface layer or surfactant layer. The direct quantitative measurement of trap concentrations in samples grown at the same temperature shows clearly that the use of a Bi surfactant layer and/or incorporating small amounts of Bi significantly improves the crystal quality, thus confirming earlier indications from RHEED oscillations monitored during MBE growth[1,18] and photoluminescence measurements.[4,5,19] Hole trap concentrations in the $10^{15}\,cm^{-3}$ range were previously reported in p-type GaAsBi Schottky diodes having 1.2 and 3.4% Bi (comparable to p-type GaAs grown at 560 °C), and it was suggested that this low trap concentration results from incorporating Bi.[20] However, to our knowledge no direct comparison of p-type GaAsBi with p-type GaAs grown at the same temperature has yet been done.

The best way to compare DLTS results for different samples is to compare their Arrhenius plots or "DLTS signatures,"[21] as is done in Fig. 5. We see that the Arrhenius plots are tightly clustered indicating that, with the exception of trap A′, the traps detected in the GaAsBi layers have emission rates similar to traps in GaAs grown at low temperatures. Therefore, these defects are unlikely to involve Bi, but instead are a result of the low growth temperature. Traps A, D, and E have the same activation energy, within the measurement error, in all the samples. However, the activation energies for traps C, C′, and B shift toward lower energy as the Bi fraction is increased (see Table II). This energy shift may be due to the lattice mismatch strain in the GaAaBi layers or to local strain due to the presence of Bi near

TABLE II. Electron trap parameters from DLTS measurements. Parameters are averages of the values measured for several diodes on each sample. The error in the activation energy is typically ±0.02 eV and about an order of magnitude for the capture cross section.

		Electron trap						
Sample	Parameter	A′	A	B	C′	C	D	E
GaAs	E_A (eV)		0.14	. . .	0.39	0.57	0.64	0.81
390 °C	σ (cm^2)		2×10^{-16}	. . .	8×10^{-14}	5×10^{-12}	1×10^{-14}	1×10^{-13}
	N_T (cm^{-3})		4×10^{14}	2×10^{14}	2×10^{15}	4×10^{15}	1×10^{16}	4×10^{15}
GaAs	E_A (eV)		0.16		0.41	[a]	. . .	[b]
330 °C	σ (cm^2)		4×10^{-16}		2×10^{-14}			
	N_T (cm^{-3})		4×10^{15}		1×10^{18}		4×10^{16}	
GaAsBi	E_A (eV)		0.16	0.26		0.47	0.65	0.79
0.3%	σ (cm^2)		5×10^{-16}	6×10^{-16}		5×10^{-14}	2×10^{-14}	2×10^{-13}
330 °C	N_T (cm^{-3})		2×10^{15}	2×10^{15}		1×10^{16}	4×10^{16}	3×10^{16}
GaAsBi	E_A (eV)	0.12	0.17	0.20		0.40	0.67	0.81
0.7%	σ (cm^2)	2×10^{-16}	1×10^{-15}	3×10^{-17}		4×10^{-15}	5×10^{-14}	2×10^{-13}
330 °C	N_T (cm^{-3})	8×10^{15}	4×10^{15}	3×10^{15}		2×10^{16}	5×10^{16}	7×10^{15}
GaAsBi	E_A (eV)	[c]	[c]	[c]	0.32	0.37	0.67	
1.1%	σ (cm^2)				2×10^{-15}	2×10^{-15}	1×10^{-13}	
330 °C	N_T (cm^{-3})				3×10^{15}	1×10^{16}	5×10^{16}	

[a]Not detected due to the very large signal from trap C′.
[b]Not measured due to high reverse bias leakage current above 400 K.
[c]No DLTS signal due to carrier freeze-out making the depletion region larger than the n-doped layer at T ≤ 200 K.

neighbors and this effect requires further investigation. We note that trap D was also the dominant trap in previously reported DLTS spectra from p-i-n diodes that have i-regions consisting of both GaAs and GaAsBi layers grown either at 350 °C (1.4%Bi) or at 310 °C (1.8%Bi).[14]

In contrast, trap A′ having activation energy 0.12 eV was detected in the sample having 0.7% Bi, but not in the sample having 0.3% Bi or in GaAs. Unfortunately, the negligible DLTS signal below ~200 K from the sample with 1.1% Bi is not indicative of the absence of defects. Due to carrier freeze-out, the depletion region extends beyond the thickness of the *n*-doped layer at these temperatures, indicating that there must be compensating acceptors in this sample. Spectra for p+/n diodes taken using a filling pulse at larger forward bias show no evidence of hole trapping. The exception is the 1.1% GaAsBi sample for which a hole trap with activation energy 1.0 eV in concentration of only 2×10^{15} cm^{-3} was detected. This suggests that the energy levels of the compensating acceptors must lie close to the valence band edge.

We now discuss possible atomic configurations of some of these traps with reference to previous work. High quality n-type GaAs layers grown by MBE at temperatures of 550–650 °C typically have defect concentrations in the 10^{12}

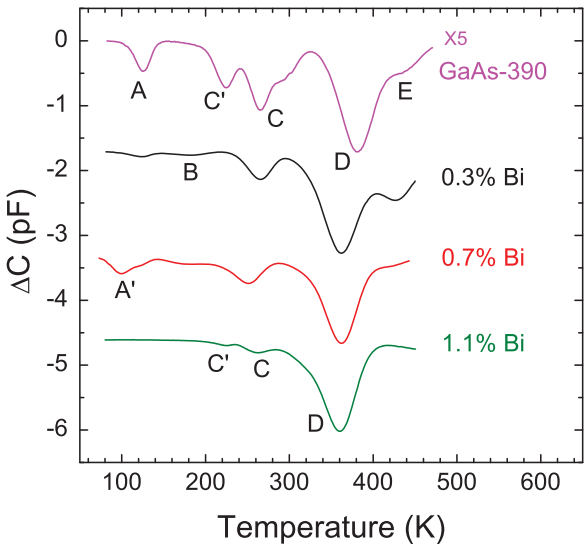

FIG. 4. DLTS spectra for three GaAsBi layers grown at 330 °C having the Bi fraction indicated and the n-type GaAs layer grown at 390 °C. The emission rate is 1163 s^{-1}. The trap filling pulse was 0.5 V forward bias for 2 ms. The steady state reverse bias voltage was 0.5 V for the GaAs layer. For the GaAsBi layers it was 2.5 V for 0.3%, 0.5 V for 0.7%, and 1.0 V for 1.1%.

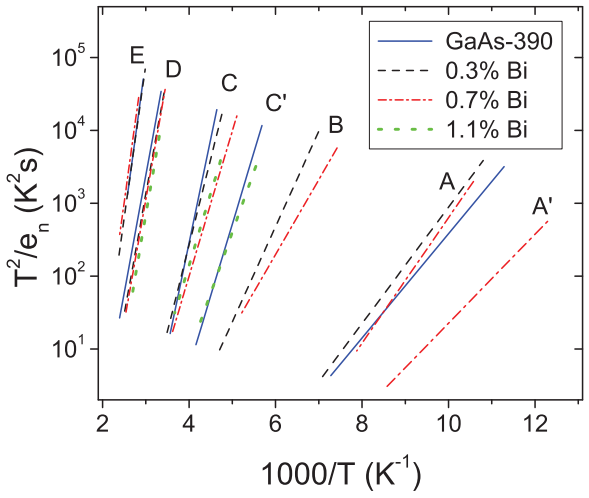

FIG. 5. Arrhenius plots comparing emission rates of traps in the GaAs sample grown at 390 °C and the three GaAsBi samples.

or $10^{13}\,cm^{-3}$ range.[16] However, at lower growth temperatures, the residence time of As adatoms on the surface increases, creating an As-rich surface, and surface atom mobility decreases as well. Thus, the concentrations of As antisite (As_{Ga}) defects are expected to be higher in GaAs layers grown at lower temperatures.

Trap E, for which the temperature of the DLTS peak was determined by fitting the spectra with a double Gaussian curve, has the same activation energy (0.80 eV) and capture cross section as the well-known EL2 trap,[21] a defect consisting of As_{Ga} with an As interstitial (As_i) neighbor.[22] The trap concentration decreases from $3 \times 10^{16}\,cm^{-3}$ in the GaAsBi 0.3% Bi layer to $5 \times 10^{15}\,cm^{-3}$ in the 0.7% Bi layer. It was not detected in the layer having 1.1% Bi.

Trap D, the dominant trap in the GaAs layer grown at 390 °C and in the GaAsBi samples with activation energy 0.65 eV, has emission energy, capture cross section, and concentration similar to a trap observed previously in GaAs layers grown by MBE at 450 °C.[13] The trap concentration is the same within the measurement error in all our samples grown at 330 °C. Since Ga vacancies, V_{Ga}, are also more likely in samples grown under As-rich conditions, this defect was suggested to be a complex consisting of both As_{Ga} and V_{Ga}.[12]

Trap A is similar to trap M1 observed in GaAs grown at standard temperatures.[16] The concentration is $2\text{-}4 \times 10^{15}\,cm^{-3}$ in the three GaAs and GaAsBi layers grown at 330 °C and is an order of magnitude lower in the GaAs layer grown at 390 °C. It is a further order of magnitude lower in the GaAs layer grown at standard conditions. Because the concentration of M1 was found to be strongly dependent on the growth temperature in the range 550–650 °C, it was suggested it is a defect complex consisting of a native defect and an impurity.[23]

Trap A′, with activation energy 0.12 eV, was observed only in the GaAsBi sample having 0.7% Bi. Since this trap is not observed in the GaAs layers or the GaAsBi layer having a lower Bi fraction, this defect may involve Bi as a constituent. We note that a bismuth antisite (Bi_{Ga}) defect was observed in Bi-doped Czochralski-grown GaAs by electron spin resonance to have the 0/+ level at 0.35-0.5 eV below the conduction band.[24]

Trap C′ is especially interesting because of its very high concentration in the GaAs layer grown under the same condition as the GaAsBi layers and its absence in the two GaAsBi layers having the lowest Bi fraction. As shown in Fig. 5, a trap having a similar emission rate appears in the 1.1% Bi GaAsBi layer. The concentration of trap C′ increased dramatically in concentration from $2 \times 10^{15}\,cm^{-3}$ in GaAs grown at 390 °C with a As/Ga atom ratio of 3 to $1 \times 10^{18}\,cm^{-3}$ in GaAs grown at 330 °C with As/Ga atom ratio of 1.7. To our knowledge this trap has not been observed previously in GaAs layers grown by MBE at these temperatures. The presence of this trap in GaAs must depend sensitively on the growth temperature and possibly also on the V/III atom ratio and As source.

We note that the layers grown at 330 °C were subsequently annealed for ~30 min. during the growth of the p+ GaAs cap layer of the p+/n junction diode structures. The GaAs layer and the 0.3% and 0.7% GaAsBi layers were annealed at 580 °C but the 1.1% GaAsBi layer was annealed at only 400 °C. The M1 defect (trap A) is found in GaAs grown at standard temperatures and is therefore stable at these annealing temperatures. Trap E (EL2) is destroyed by rapid quenching of GaAs from 950 °C, but it is stable at lower temperatures.[25] The thermal stability of the other electrons traps in not known. However, since traps C′, C, and D are observed in the GaAs and GaAsBi layers grown at 330 °C, and subsequently, annealed at 580 °C, these traps appear to be stable at this temperature. A systematic annealing study of GaAsBi layers in this alloy composition range has not been published. An annealing study including DLTS together with optical and structural measurements would be desirable.

CONCLUSION

We have investigated n-type GaAs and dilute GaAsBi layers grown by MBE at temperatures below 400 °C. DLTS spectra show that incorporating <1% Bi suppresses the formation of an electron trap with activation energy 0.40 eV, thus reducing the total trap concentration in dilute GaAsBi layers by more than a factor of 20. Otherwise, we find the same traps in these dilute GaAsBi layers as in GaAs grown at the same temperature. For example, the dominant traps are defect complexes involving As_{Ga}, as expected for MBE growth at these temperatures. Trap concentrations in GaAs grown by MBE at these temperatures depend sensitively on the growth conditions suggesting that trap concentrations in GaAsBi may be reduced by optimizing the growth parameters.

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APPENDIX

Here, we modify Eqs. (2) and (3) for the case of a deep level in a semiconductor with two donor levels. These modifications are needed to calculate the concentration of the D trap level from the DLTS spectrum of the GaAs sample grown at 330 °C. The apparent doping concentration, obtained from the C-V curves measured at the temperature, where the D trap signal is observed in Figure 3, can be interpreted as the total density of the Si dopant atoms and the C′ trap centers. The latter are thus donors having a concentration of $10^{18}\,cm^{-3}$ (see Table II), i.e., a factor 10 larger than the nominal Si dopant concentration of about $10^{17}\,cm^{-3}$, shown in Table I. Therefore, the calculation of the D trap density in the 330 °C GaAs sample requires that both the shallow donor concentration at the Si level ($E_D = E_C - 5\,meV$) and the deep donor density at the C′ trap level ($E_{C'} = E_C - 0.41\,eV$) are taken into account in Eqs. (2) and (3).

When two donor levels respond to the capacitance-measurement test signal, the depletion width, W, obtained from the reciprocal of the capacitance C (here, C is the

capacitance per unit area), $W = \varepsilon/C$, is the average of the depletion widths of the two donor levels.[17] Specifically

$$W = \frac{N_1 W_1 + N_2 W_2}{N_1 + N_2}, \tag{A1}$$

where W_1 and W_2 are the depletion widths for the shallow and deep donor levels (see Figure 2) having concentrations N_1 and N_2, respectively. This result is valid for a Schottky diode or a one-sided abrupt junction diode for which the depletion width on the heavily doped side is negligible.[26] By substituting $W_2 = W_1 - \lambda(C')$ in Eq. (A1), where $\lambda(C') = 70\,\text{nm}$ is obtained from Eq. (3) with $N_d = N_1 = 10^{17}\,\text{cm}^{-3}$, $E_T = E_{C'}$ and $E_F = E_C - 60\,\text{meV}$ is the Fermi energy in the bulk semiconductor with $N_2 = 10^{18}\,\text{cm}^{-3}$, we can calculate W_1 and W_2 as functions of W. In this case, Eq. (3) cannot be applied to calculate $\lambda(D)$ because it neglects the space charge N_2 at the ionized C' donor level, as explained above.

The value of $\lambda(D)$ can be obtained as the value of the depletion width W_2, when $E_F = E_C - E_T = 0.64\,\text{eV}$ at the junction. Specifically, we can write

$$E_F - E_T = \frac{e^2}{2\varepsilon} \times \{N_1 \times [\lambda(C') + \lambda(D)]^2 + N_2 \times \lambda(D)^2\}, \tag{A2}$$

where we have set $W_2 = \lambda(D)$ and $W_1 = \lambda(D) + \lambda(C')$. It then follows that:

$$\lambda(D) = \frac{-N_1 \times \lambda(C') + \sqrt{N_1{}^2 \times \lambda(C')^2 - (N_1 + N_2) \times \left[N_1 \times \lambda(C')^2 - (2\varepsilon/e^2) \times (E_F - E_T)\right]}}{N_1 + N_2}. \tag{A3}$$

Equation (A3) replaces Eq. (3) for the case of the D trap level. Specifically, for $E_F = E_C - 60\,\text{meV}$ and for the D trap energy $E_T = E_C - 0.64\,\text{eV}$, we obtain $\lambda(D) = 11.5\,\text{nm}$. Therefore, the potential drop across the charge trapped at the D center, which appears in the denominator of Eq. (2), is proportional to $W_2 - \lambda(D)$, at all biases.

The numerator of Eq. (2) is proportional to the potential drop across the space charge at the ionized donors. In the case of two donor levels, as for the 330 °C GaAs sample, Eq. (2) can thus be written as

$$N_T(D) = 6 \left|\frac{\Delta C}{C(V_R)}\right| \frac{N_1 \times [\lambda(C') + W_2(V_R)]^2 + N_2 \times W_2(V_R)^2}{[W_2(V_R) - \lambda(D)]^2 - [W_2(V_P) - \lambda(D)]^2}, \tag{A4}$$

which yields $N_T(D) = 4.4 \times 10^{16}\,\text{cm}^{-3}$ for the 330 °C GaAs sample. In this diode, the p+ doping level of $3 \times 10^{18}\,\text{cm}^{-3}$ is only three times larger than the total donor density on the n side of the junction. Therefore, the error in the trap concentration is about 25%.

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